

**DIGITAL ELECTRONICS PRACTICAL -1.**

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**Practical 1: Introduction to VHDL.**

VHDL stands for very high-speed integrated circuit hardware description language. It is a programming language used to model a digital system by dataflow, behavioral and structural style of modeling. This language was first introduced in 1981 for the department of Defense (DoD) under the VHSIC program.

Describing a Design

In VHDL an entity is used to describe a hardware module. An entity can be described using,

*• Entity declaration*

*• Architecture*

*• Configuration*

*• Package declaration*

*• Package body*

Entity Declaration

It defines the names, input output signals and modes of a hardware module.

**Syntax** −

|  |
| --- |
| entity entity\_name is  Port declaration;  end entity\_name; |

An entity declaration should start with ‘entity’ and end with ‘end’ keywords. The direction will be input, output or inout.

|  |  |
| --- | --- |
| In | Port can be read |
| Out | Port can be written |
| Inout | Port can be read and written |
| Buffer | Port can be read and written, it can have only one source. |

**Architecture** −

Architecture can be described using structural, dataflow, behavioral or mixed style.

**Syntax** −

|  |
| --- |
| architecture architecture\_name of entity\_name  architecture\_declarative\_part;  begin  Statements;  end architecture\_name; |

Here, we should specify the entity name for which we are writing the architecture body. The architecture statements should be inside the ‘begin’ and ‘énd’ keyword. Architecture declarative part may contain variables, constants, or component declaration.

**Data Flow Modeling**

In this modeling style, the flow of data through the entity is expressed using concurrent (parallel) signal. The concurrent statements in VHDL are WHEN and GENERATE.

Besides them, assignments using only operators (AND, NOT, +, \*, sll, etc.) can also be used to construct code.

Finally, a special kind of assignment, called BLOCK, can also be employed in this kind of code.

In concurrent code, the following can be used −

*• Operators*

*• The WHEN statement (WHEN/ELSE or WITH/SELECT/WHEN); • The GENERATE statement;*

*• The BLOCK statement*

**Behavioral Modeling**

In this modeling style, the behavior of an entity as set of statements is executed sequentially in the specified order. Only statements placed inside a PROCESS, FUNCTION, or PROCEDURE are sequential.

PROCESSES, FUNCTIONS, and PROCEDURES are the only sections of code that are executed sequentially.

However, as a whole, any of these blocks is still concurrent with any other statements placed outside it.

One important aspect of behavior code is that it is not limited to sequential logic. Indeed, with it, we can build sequential circuits as well as combinational circuits.

The behavior statements are IF, WAIT, CASE, and LOOP. VARIABLES are also restricted and they are supposed to be used in sequential code only. VARIABLE can never be global, so its value cannot be passed out directly.

**Structural Modeling**

In this modeling, an entity is described as a set of interconnected components. A component instantiation statement is a concurrent statement. Therefore, the order of these statements is not important. The structural style of modeling describes only an interconnection of components (viewed as black boxes),

without implying any behavior of the components themselves nor of the entity that they collectively represent.

In Structural modeling, architecture body is composed of two parts − the declarative part (before the keyword begin) and the statement part (after the keyword begin).

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